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Fig. 1

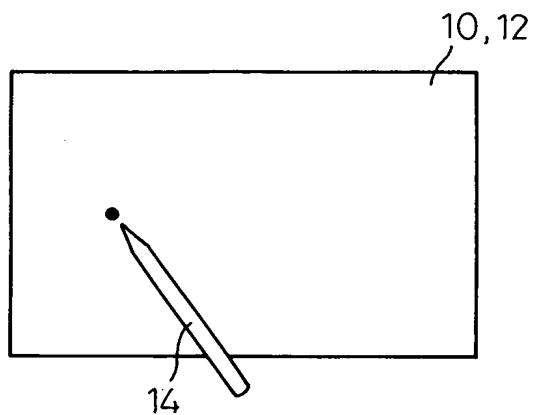


Fig. 2

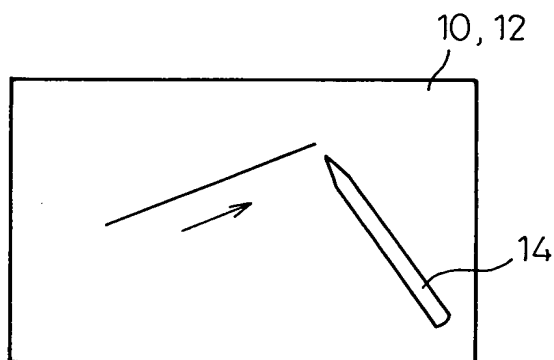
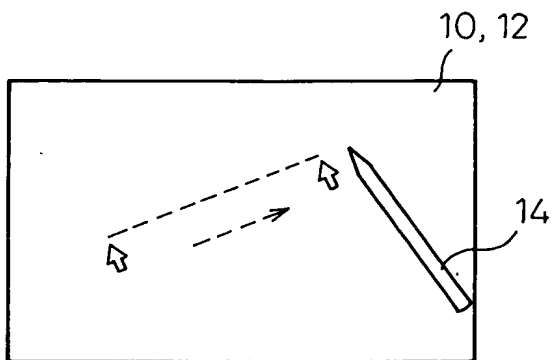


Fig. 3



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Fig. 4

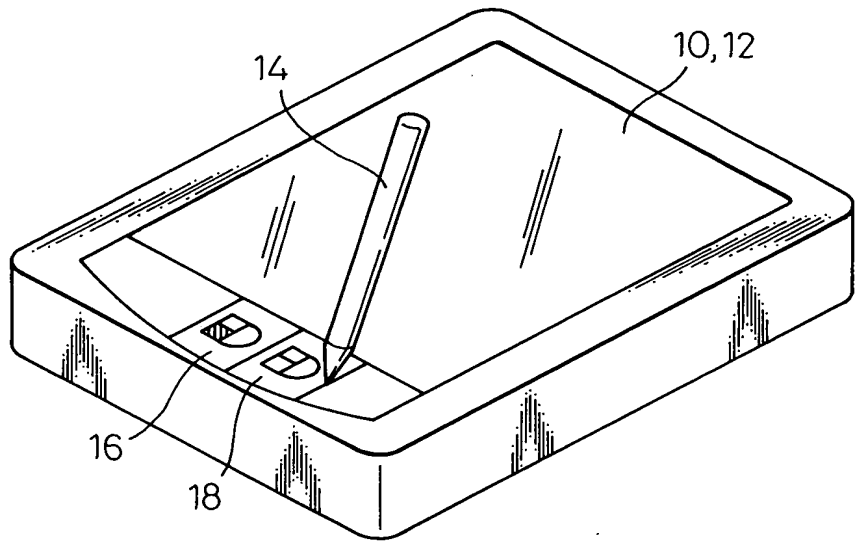
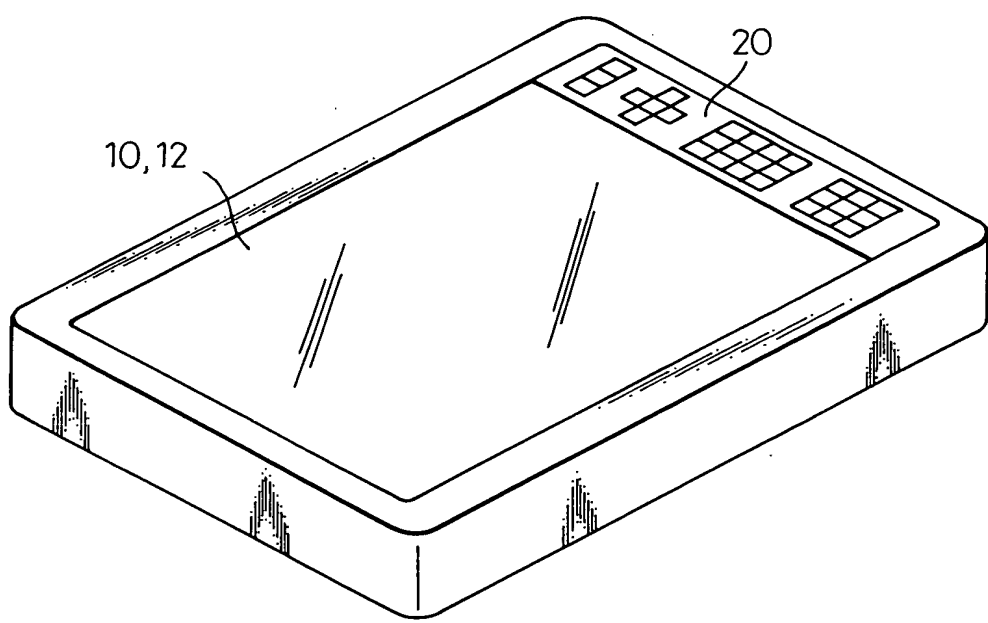


Fig. 5



APPROVED	O.G. FIG.	
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Fig. 6A

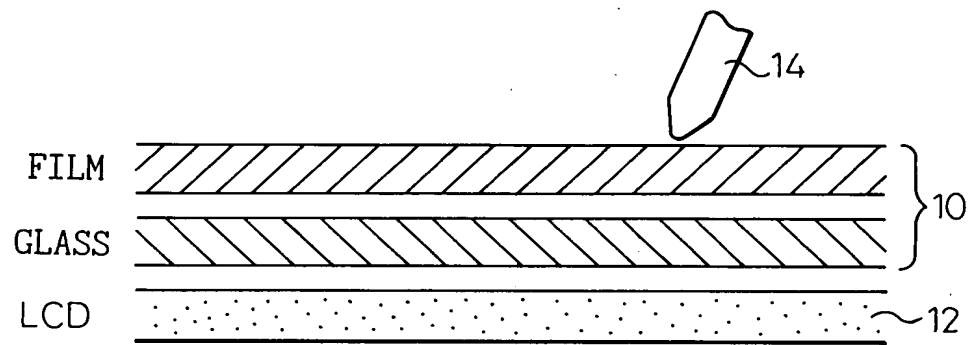
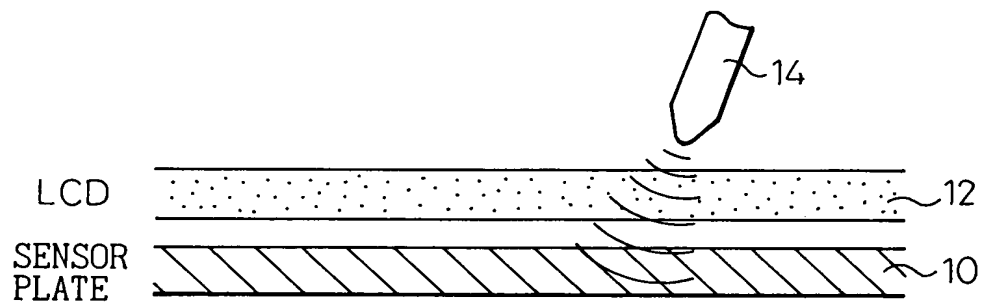


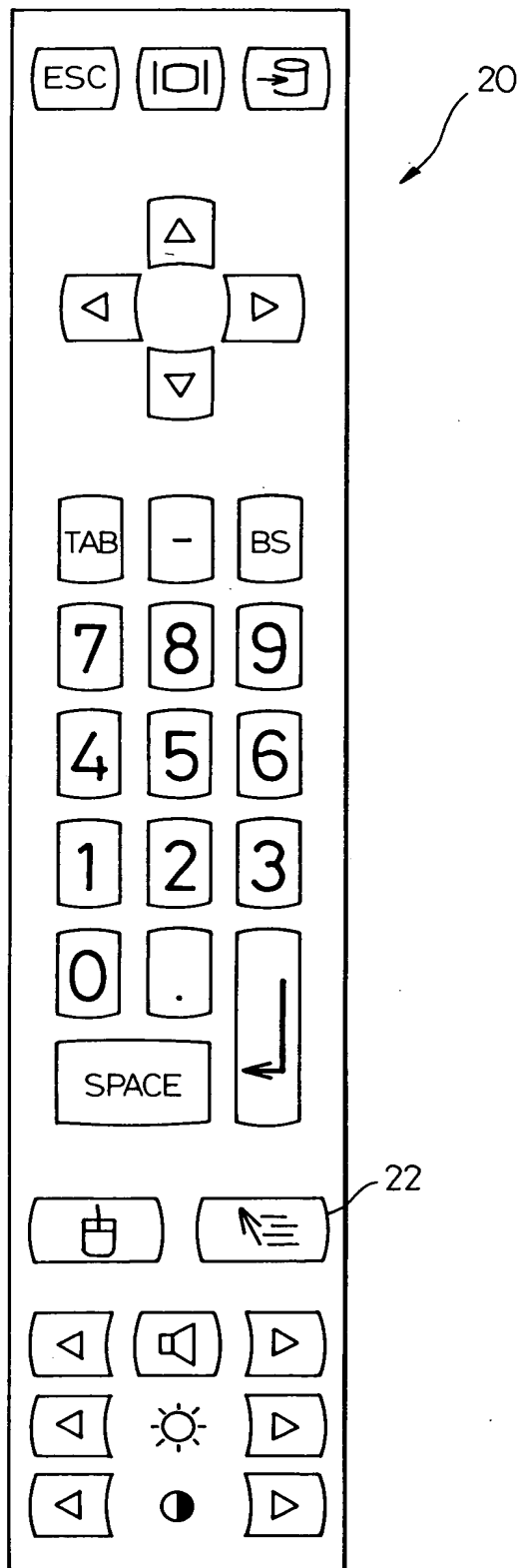
Fig. 6B



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Fig. 7



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Fig. 8

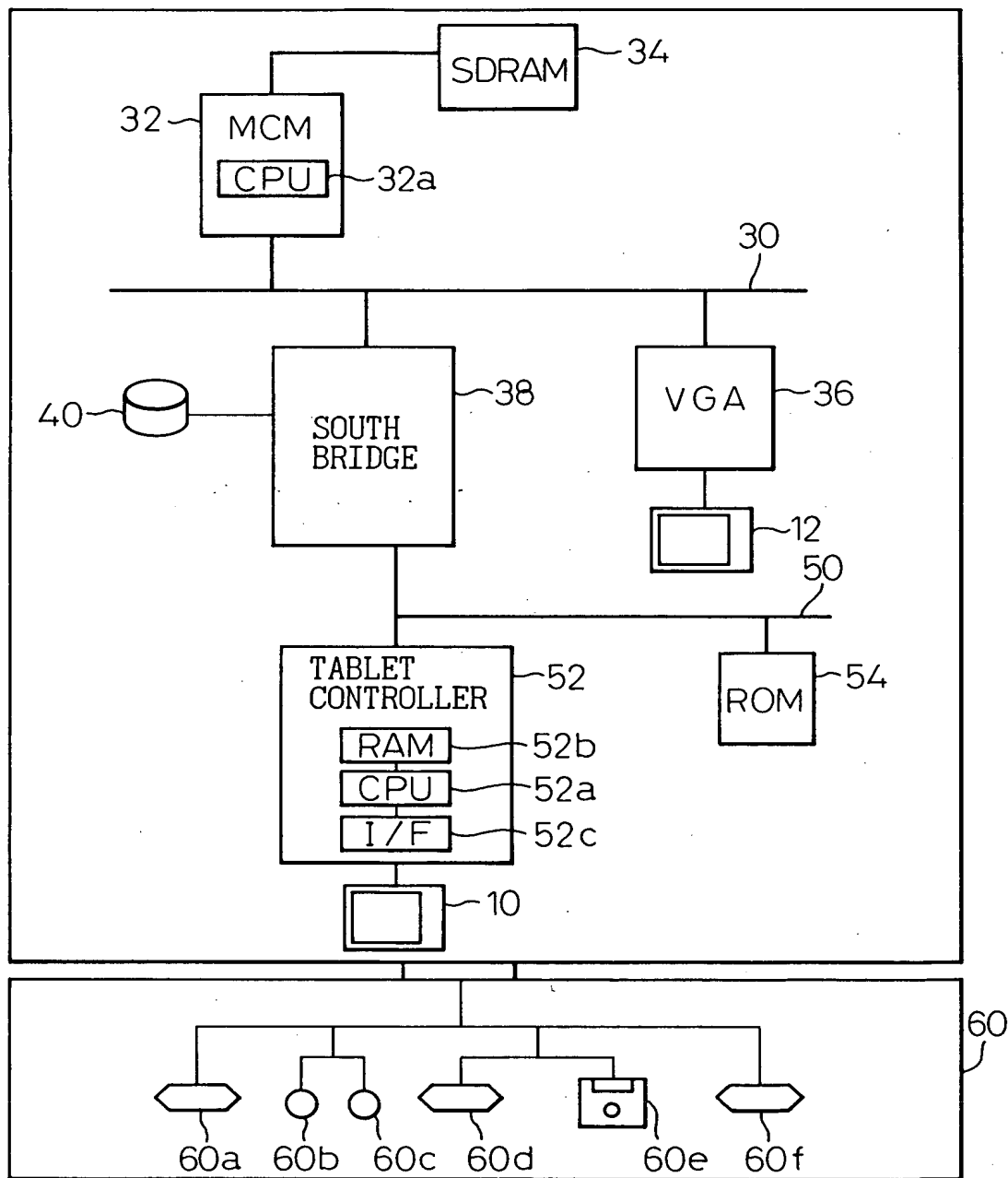
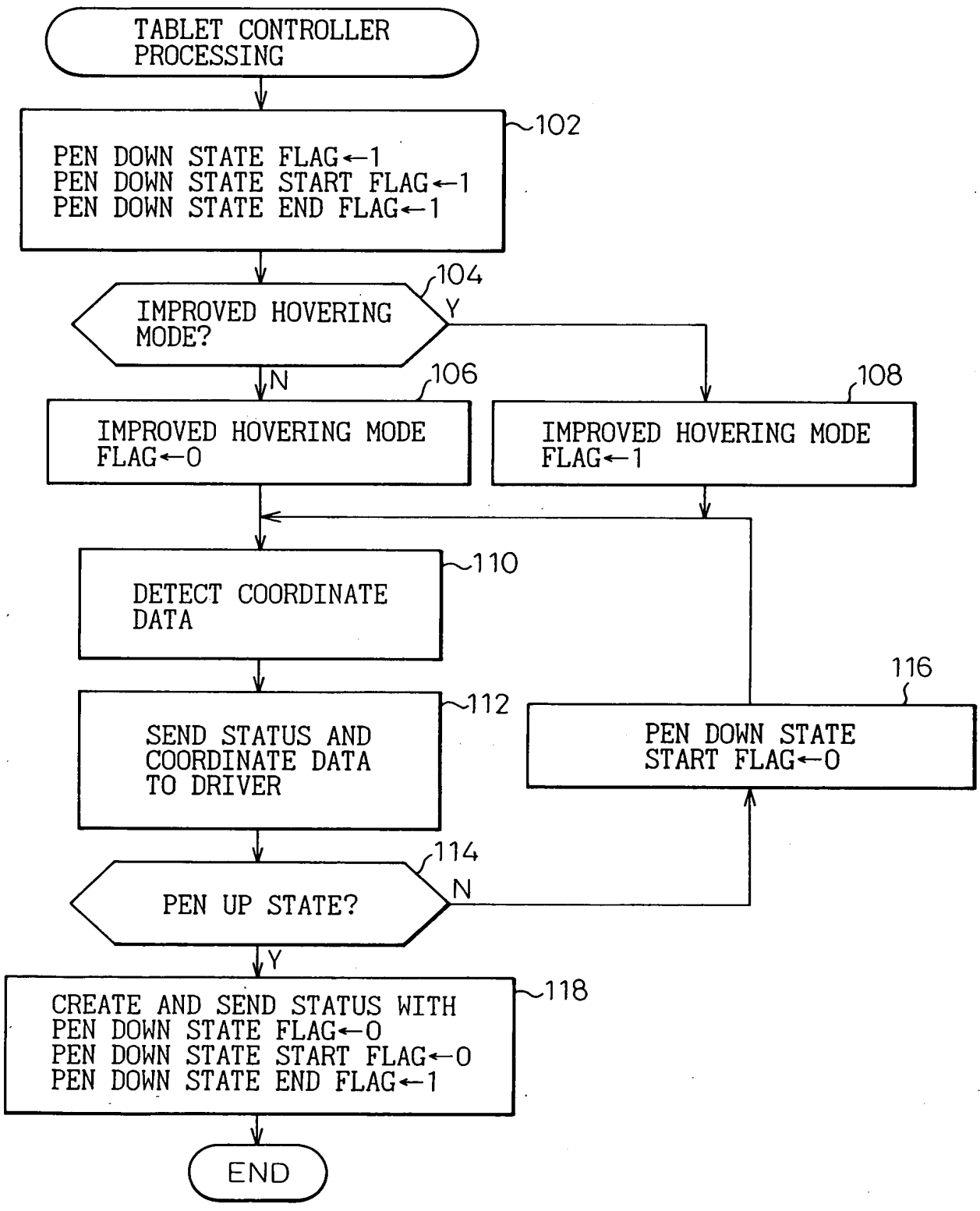
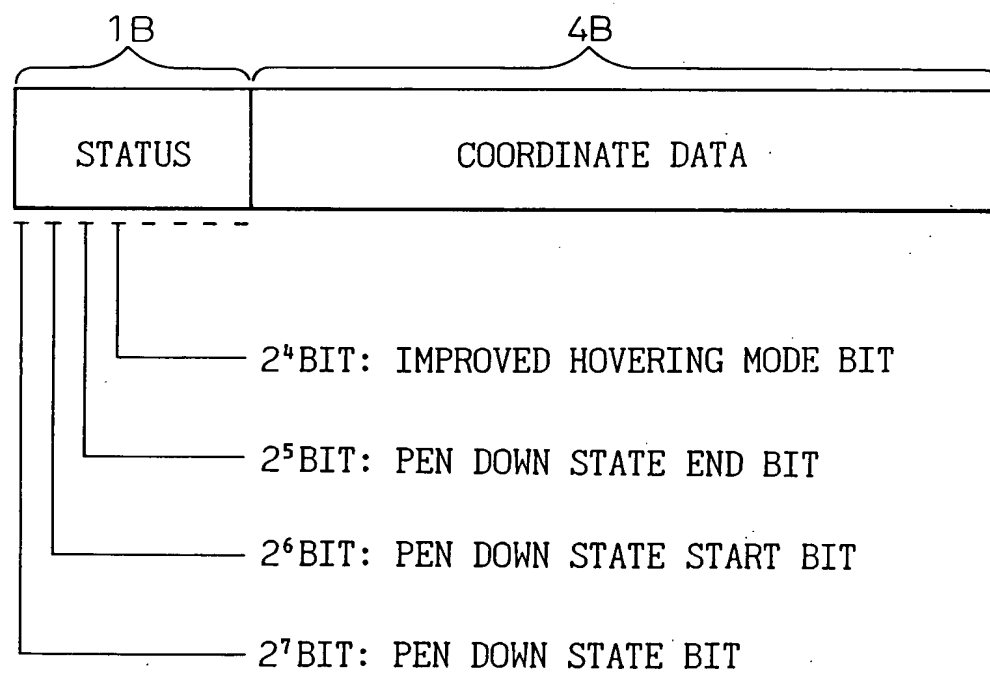


Fig. 9



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Fig.10



APPROVED	O.G. FIG.	
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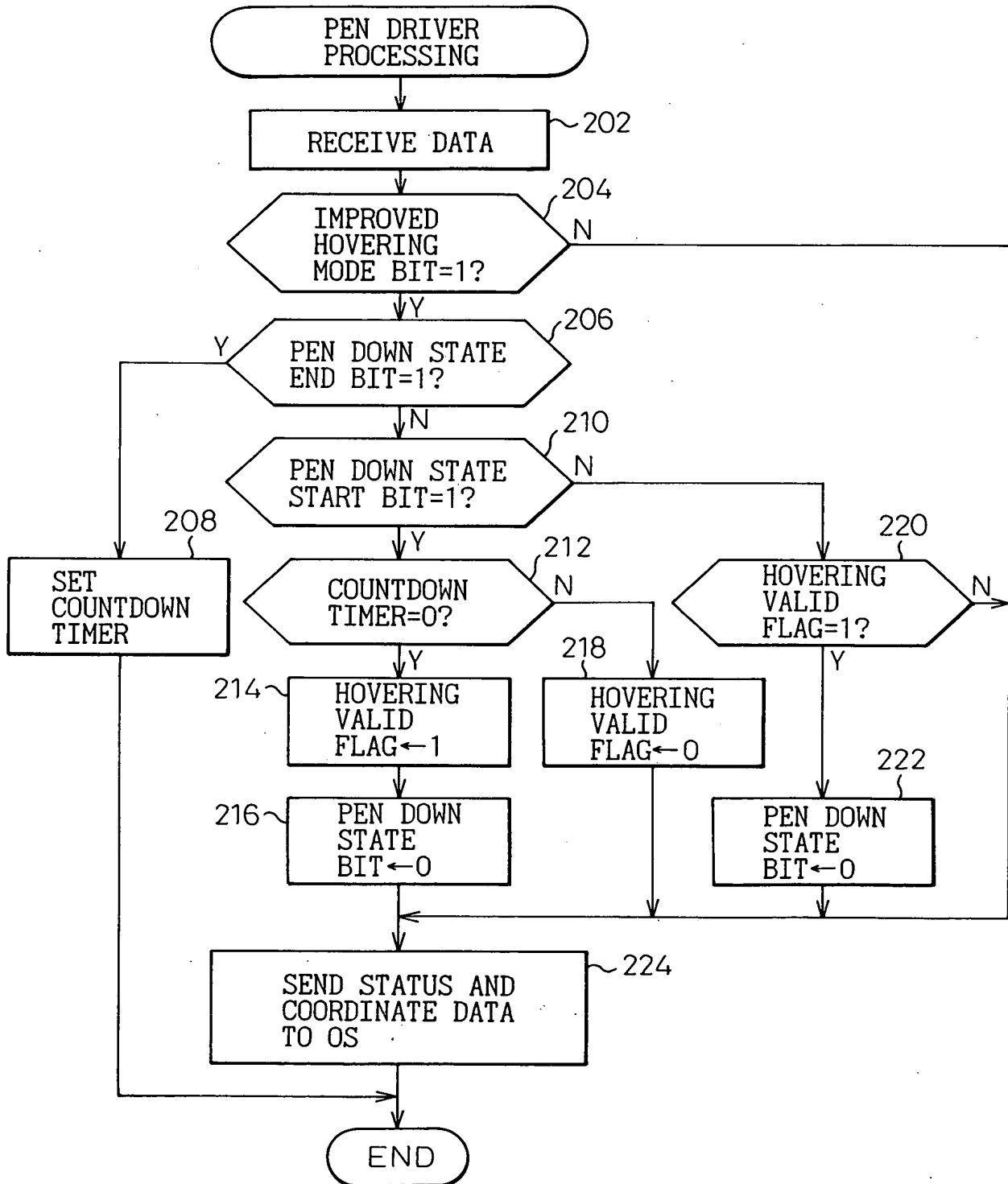
Fig. 11

CASE	STEPS CARRIED OUT	PEN DOWN STATE FLAG	PEN DOWN STATE START FLAG	PEN DOWN STATE END FLAG	IMPROVED HOVERING MODE FLAG
(A) PEN DOWN STATE IS FIRST ENTERED	102,104, 108,110, 112	1	1	0	1
(B) DURING PEN DOWN STATE	LOOP OF 114,116, 110,112	1	0	0	1
(C) PEN UP IS DETECTED	114,118	0	0	1	1



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Fig. 12



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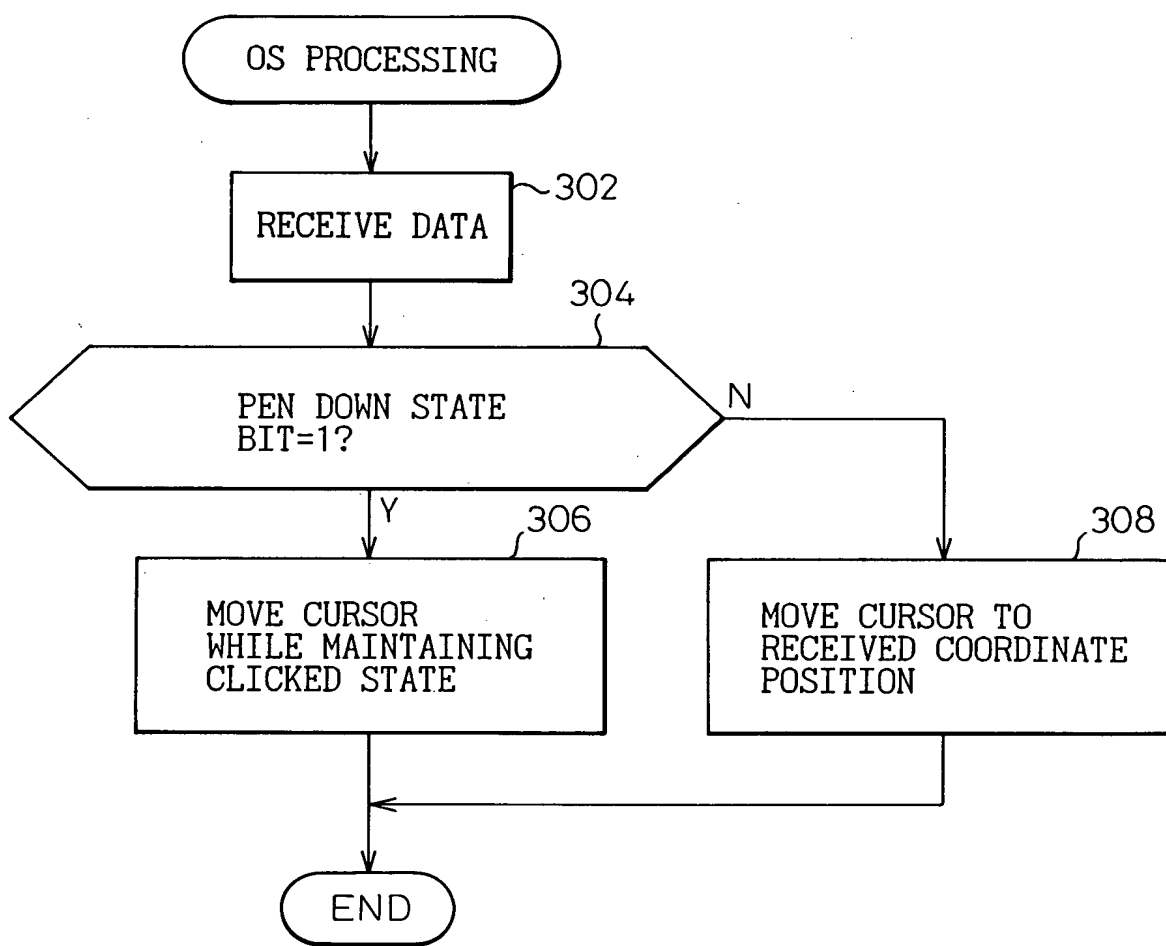
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Fig. 13

CASE		PEN DOWN STATE BIT	PEN DOWN STATE START BIT	PEN DOWN STATE END BIT	HOVERING VALID FLAG	STEPS CARRIED OUT	HOVERING VALID FLAG AFTER COMPLETION OF PROCESSING	PEN DOWN STATE BIT AFTER COMPLETION OF PROCESSING
(A)	FINAL STATUS IS RECEIVED	0	0	1	-	202,204,206, 208	-	-
(B)	FIRST STATUS IS RECEIVED WITH TIMER=0	1	1	0	-	202,204,206, 210,212,214, 216,224	1	0
(C)	INTERMEDIATE STATUS IS RECEIVED FOLLOWING (B)	1	0	0	1	202,204,206, 210,220,222, 224	1	0
(D)	FIRST STATUS RECEIVED WITH TIMER≠0	1	1	0	-	202,204,206, 210,212,218, 224	0	1
(E)	INTERMEDIATE STATUS IS RECEIVED FOLLOWING (D)	1	0	0	0	202,204,206, 210,220,224,	0	1

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Fig.14



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Fig .15A

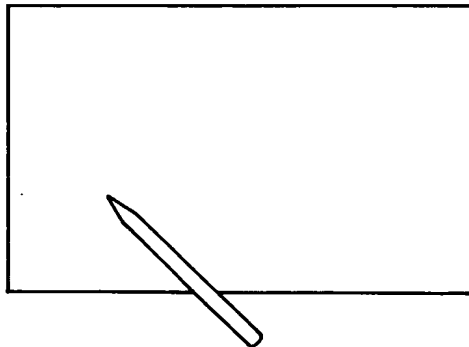


Fig .15B

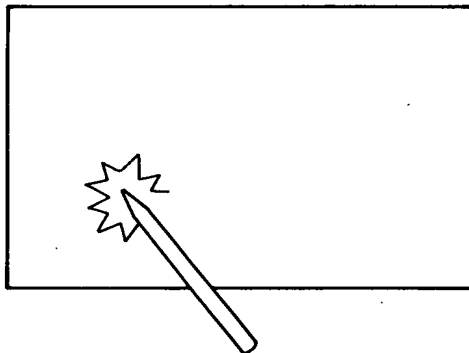


Fig .15C

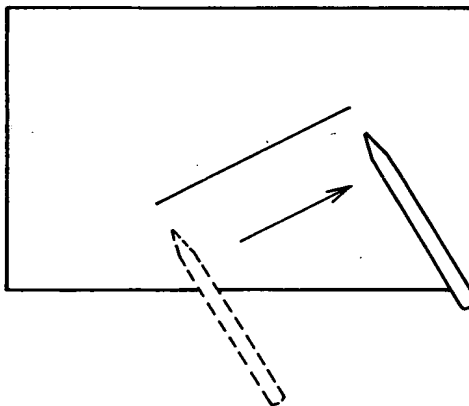


Fig.16A  
PRIOR ART

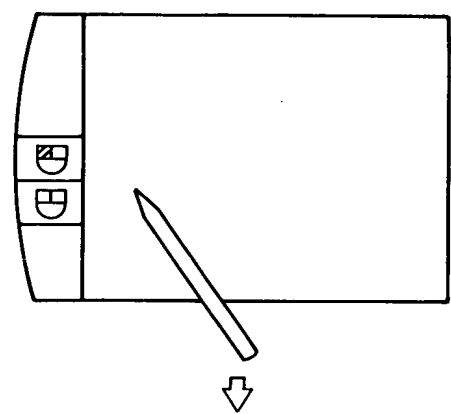


Fig.16B  
PRIOR ART

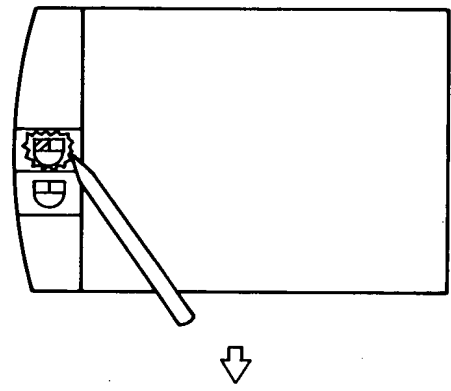


Fig.16C  
PRIOR ART

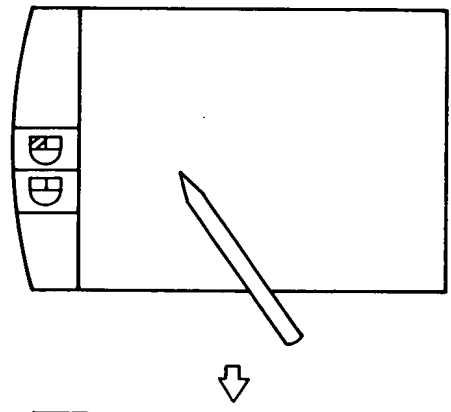
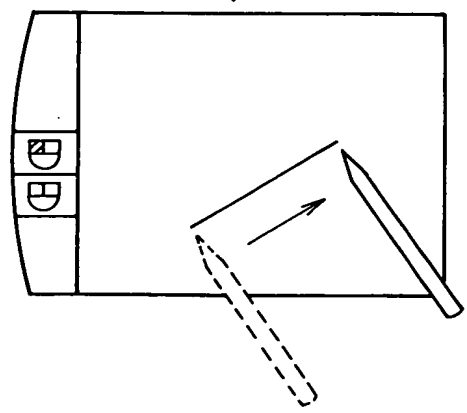


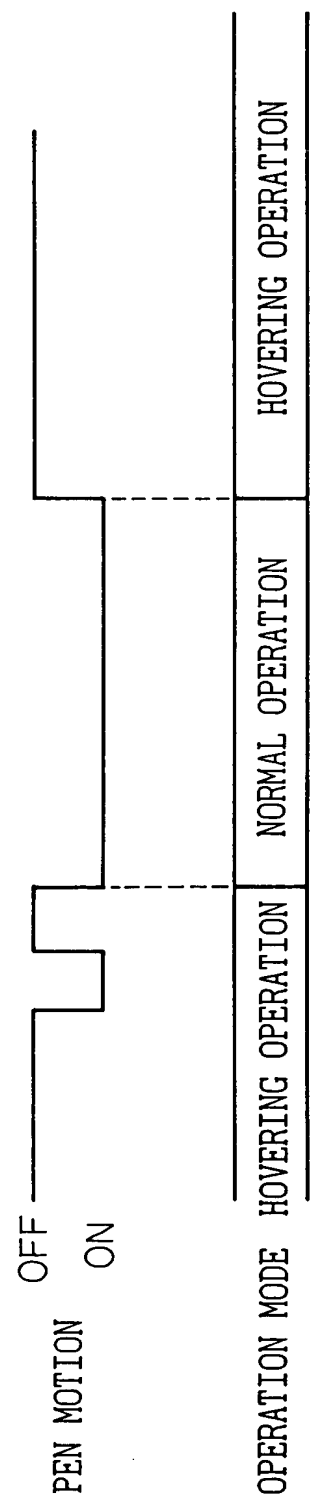
Fig.16D  
PRIOR ART



APPROVED	O.G. FIG.	
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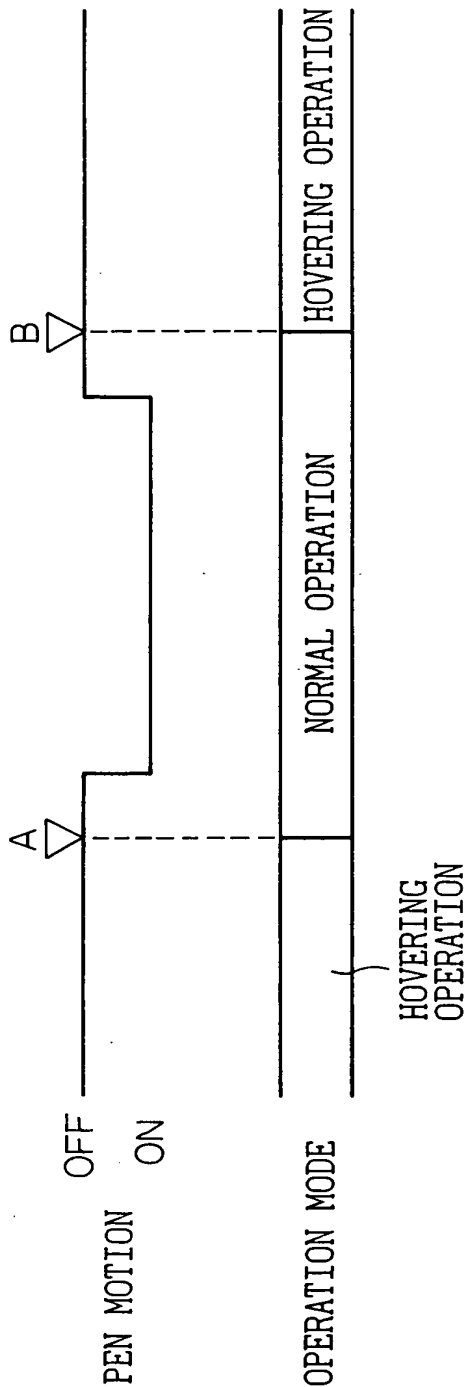
Fig.17



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

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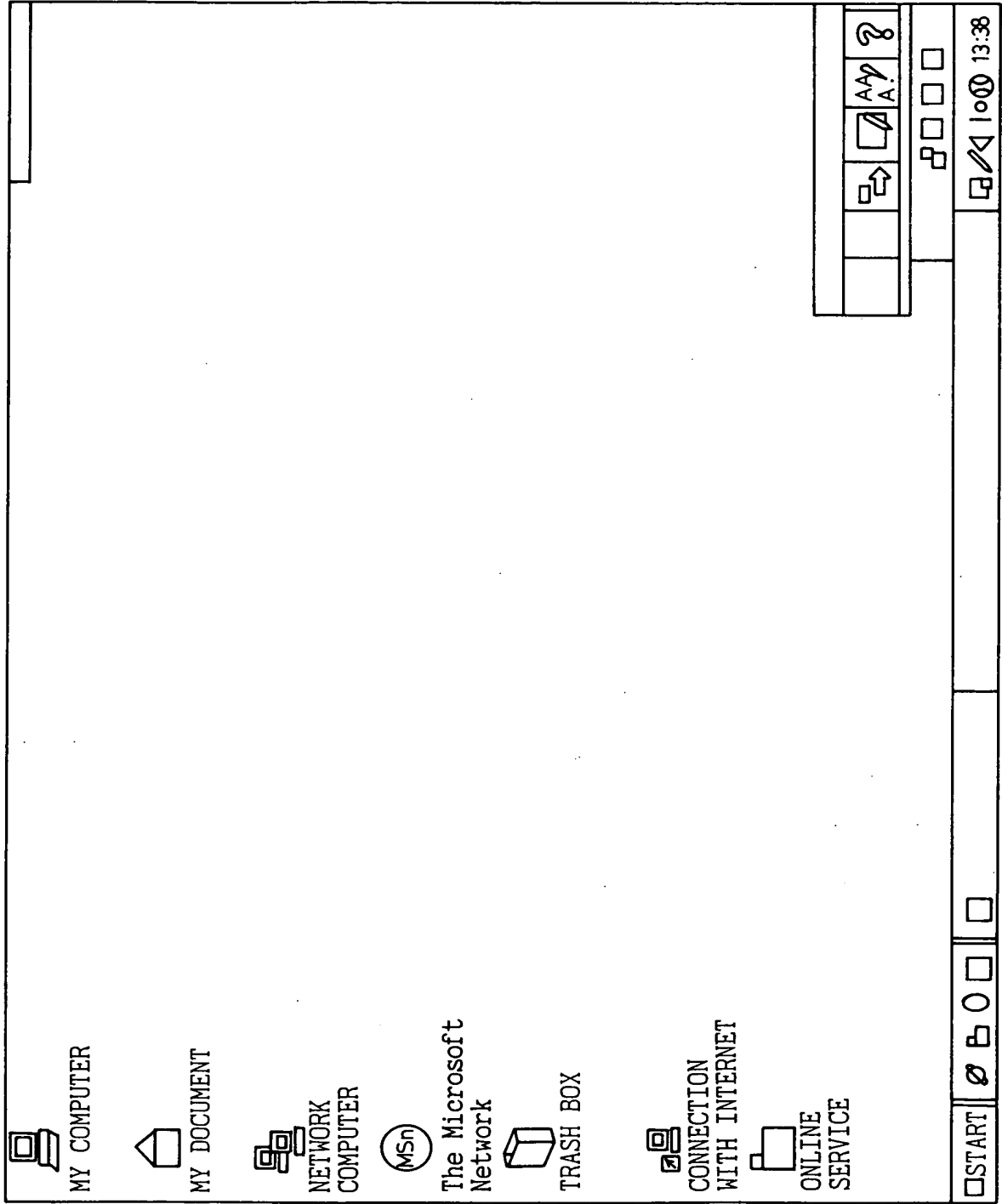
Fig.18  
PRIOR ART



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Fig.19





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Fig. 20A

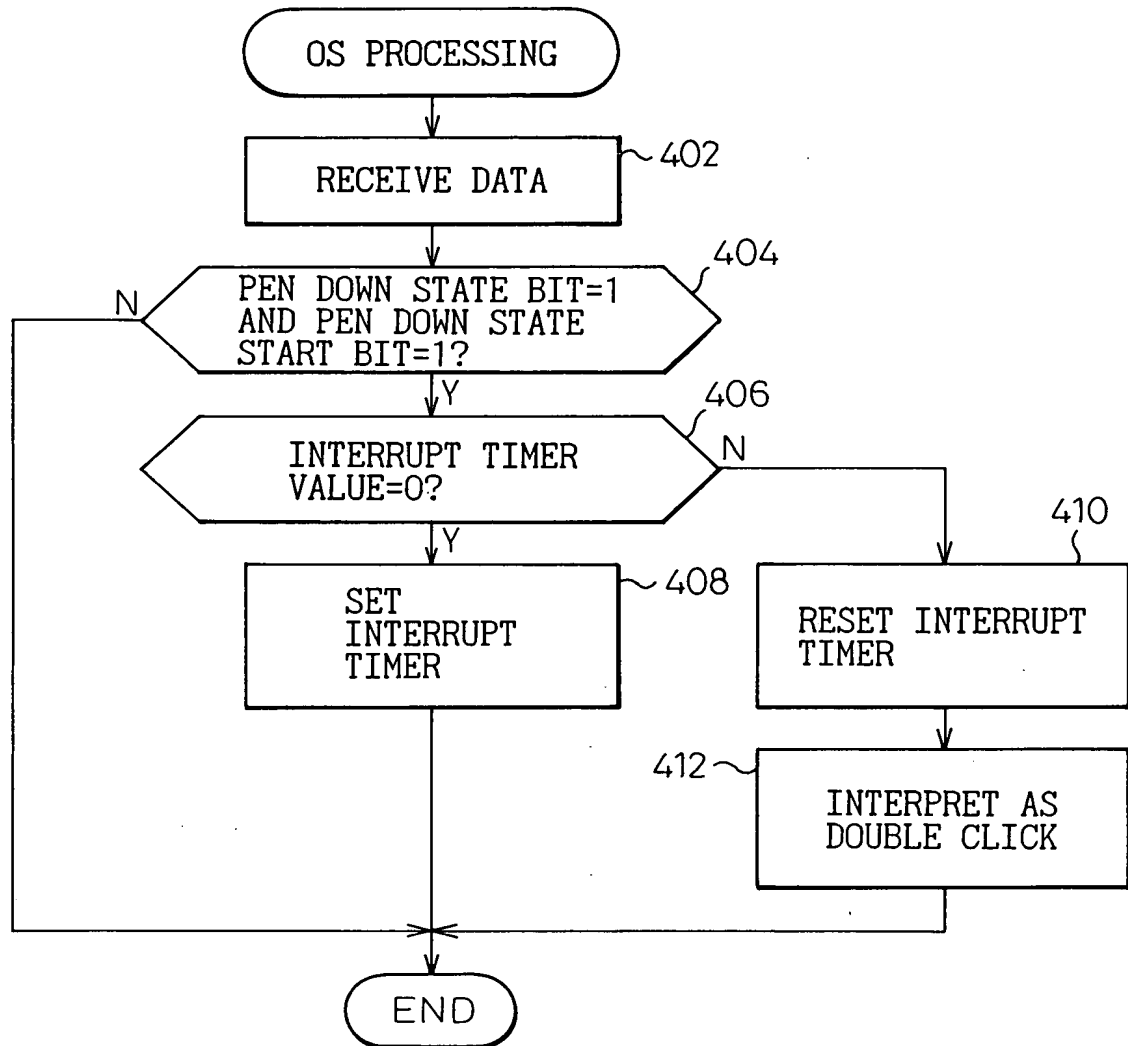


Fig. 20B

